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09/817,058	03/27/2001	Hitoshi Tada	401142	9201

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EXAMINER
ARTMAN, THOMAS R

ART UNIT	PAPER NUMBER
2882	

DATE MAILED: 05/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/817,058	TADA ET AL.	
	Examiner	Art Unit	
	Thomas R Artman	2882	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *18-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terakado (JP 0326338 A) and in view of Sano (US 5,339,370).

Regarding claim 1, Terakado teaches the structure of a ridge waveguide optical modulator (Fig.1), including:

1) a semi-insulating semiconductor substrate (item 1) with a principal plane including a partially exposed surface,

2) an optical waveguide ridge disposed on the substrate that includes;

a) a first cladding layer of a first conductivity type (item 2),

b) an optical absorption layer (item 3), and

c) a second cladding layer of a second conductivity type (item 4),

3) the ridge has a side with a flat portion extending uniformly from the top of the ridge to the exposed surface of the semiconductor substrate,

4) a dielectric film (item 10) which covers the ridge and the substrate and which has a first opening at the top of the ridge and a second opening in a region of the substrate other than the exposed surface,

5) a first electrode (item 14) disposed on the dielectric film and mounted through the first opening on the top of the ridge and having one end on the substrate at the exposed surface, and

6) a second electrode disposed on the semiconductor substrate and connected to the first cladding layer through the second opening in the dielectric film.

Terakado does not disclose the first electrode being extended along the flat side of the ridge waveguide and in contact with the dielectric film.

Sano teaches the practice of a first electrode that is in contact with the dielectric film throughout its extension along the flat portion of the ridge waveguide.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the electrode extension in contact with the dielectric layer because it is far easier to manufacture, with fewer steps for depositing and then etching the sacrificial layer that allows formation of the "air bridge."

With respect to claims 3, 5 and 11, Terakado discloses the extension of the first cladding layer away from the ridge waveguide in order to contact the second electrode through the second opening of the dielectric layer.

Claims 2, 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terakado and Sano and in view of Yamanishi (US 5,173,955).

Regarding claim 2, Terakado and Sano do not teach the practice of extending the first electrode over both sides of the ridge waveguide. Yamanishi teaches such a structure in Fig.11, item 46.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that having an electrode on one side, as shown in Terakado and Sano, or having the electrode on both sides of the ridge waveguide are functional equivalents, both performing the function of simplified wiring and access to the second cladding layer.

Regarding claims 4 and 6, Terakado discloses the extension of the first cladding layer away from the ridge waveguide in order to contact the second electrode through the second opening of the dielectric layer.

Claims 1, 3, 5, 7, 9 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano and in view of Soref (US 5,838,870) and Huang (US 6,222,951).

Regarding claim 1, Sano teaches a MQW ridge waveguide optical modulator (Fig.2A), including:

1) a semi-insulating semiconductor substrate (item 7) with a principal plane including a partially exposed surface,

2) an optical waveguide ridge disposed on the substrate that includes;

a) a first cladding layer of a first conductivity type (item 5-2),

b) an optical absorption layer (item 3), and

c) a second cladding layer of a second conductivity type (item 5-1),

3) the ridge has a side with a flat portion extending uniformly from the top of the ridge to the exposed surface of the semiconductor substrate,

4) a dielectric film (items 9-1 and 9-2) which covers the ridge and the substrate and which has a first opening at the top of the ridge,

5) a first electrode (item 10) disposed on the dielectric film and mounted through the first opening on the top of the ridge, extending on the flat portion of the side of the ridge while in contact with the dielectric layer, and having one end on the substrate at the exposed surface, and

6) a second electrode disposed on the semiconductor substrate.

Sano does not teach a second opening in the dielectric layer in a substrate surface region excluding the exposed surface region or a connection of the second electrode with the first cladding layer through the second opening in the dielectric layer.

Soref teaches of a ridge waveguide (Fig.2e) where a second opening in the outer dielectric layer allows the second electrode to contact the first cladding layer, rather than using a body contact on the underside of the substrate as taught by Sano. Soref further states that this method allows convenient access to the first cladding layer. Other advantages would be readily recognized by those skilled in the art, such as faster switching times, lower operating voltages, and simpler electrical connections. Soref does not teach the position of the opening to be on the substrate region.

Huang teaches the use of body electrodes being formed on the top of a substrate region through openings in the dielectric layer (Fig.3, contacting lower cladding layer 42 for modulator 50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the second electrode in contact with the first cladding layer on the substrate region. The placement of the second electrode on the same side of the substrate as the ridge

waveguide provides simple, convenient electrical connection to the first cladding layer. Further, the teachings of Soref and Huang demonstrate obvious functional equivalents relating to the exact placement of the electrode, either making contact on top of the substrate region or along the side of the waveguide ridge. In either configuration, both make contact through an opening in the dielectric layer.

With respect to claims 3 and 11, all three references disclose extensions of the first cladding layer beyond the ridge waveguide region (Fig.1A in Sano, Fig.2e in Soref, and Fig.3 in Huang). Particularly in Soref and Huang, the extensions are used specifically to contact the second electrode, where the electrode is mounted through the second opening.

With regards to claim 5, both Soref and Huang disclose the second electrode making contact to the extended portion of the first cladding layer through the second opening in the dielectric layer.

In regards to claims 7 and 9, Soref teaches the practice of providing a dielectric layer between the substrate and the first cladding layer of the ridge waveguide (Fig.2e). Soref teaches the use of silicon on insulator (SOI) and related technologies that are well known in the art for improving electrical isolation between devices on a common substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place a dielectric layer between the substrate and the lower cladding layer for improved electrical isolation between the ridge waveguide and other devices on the same substrate.

Claims 12 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano, Soref and Huang and in view of Yamada (US 6,374,028).

Regarding both claims, Sano, Soref and Huang do not teach the use of an additional high-resistance layer between the ridge waveguide side and the dielectric layer. Yamada teaches the practice of adding a high-resistance layer in such a location in Fig.7, and as described in part in col.5, line 27, to col.6, line 5. Particularly in lines 47-64, the additional layer 23 is a high-resistance layer between the ridge waveguide side and the outer dielectric layer, item 20. It provides better optical mode control in the waveguide while keeping the operating capacitance of the entire waveguide to a minimum. In this way, high switching speeds can be achieved.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a high-resistance layer between the side of the ridge waveguide and the dielectric layer for improved optical mode propagation control while keeping a minimal capacitance of the waveguide for faster switching speeds.

Claims 2, 4, 6, 8 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano, Soref and Huang, and in view of Yamanishi.

Regarding claim 2, none of Sano, Soref and Huang disclose the practice of placing a first electrode over both sides of the ridge waveguide and having ends on the substrate. Yamanishi teaches such a structure in Fig.11, item 46.

It would have been obvious to one of ordinary skill in the art at the time the invention was made that having an electrode on one side, as shown in the three previous cited references,

or having the electrode on both sides of the ridge waveguide are functional equivalents, both performing the function of simplified wiring and access to the second cladding layer.

With respect to claim 4, Sano, Soref and Huang disclose extensions of the first cladding layer beyond the ridge waveguide region (Fig.1A in Sano, Fig.2e in Soref, and Fig.3 in Huang). Particularly in Soref and Huang, the extensions are used specifically to contact the second electrode, where the electrode is mounted through the second opening.

With regards to claim 6, both Soref and Huang disclose the second electrode making contact to the extended portion of the first cladding layer through the second opening in the dielectric layer.

In regards to claims 8 and 10, Soref teaches the practice of providing a dielectric layer between the substrate and the first cladding layer of the ridge waveguide (Fig.2e). Soref teaches the use of silicon on insulator (SOI) and related technologies that are well known in the art for improving electrical isolation between devices on a common substrate. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to place a dielectric layer between the substrate and the lower cladding layer for improved electrical isolation between the ridge waveguide and other devices on the same substrate.

Claims 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano, Soref, Huang and Yamanishi, and in view of Yamada.

Regarding both claims, Sano, Soref, Huang and Yamanishi do not teach the use of an additional high-resistance layer between the ridge waveguide side and the dielectric layer. Yamada teaches the practice of adding a high-resistance layer in such a location in Fig.7, and as described in part in col.5, line 27, to col.6, line 5. Particularly in lines 47-64, the additional layer 23 is a high-resistance layer between the ridge waveguide side and the outer dielectric layer, item 20. It provides better optical mode control in the waveguide while keeping the operating capacitance of the entire waveguide to a minimum. In this way, high switching speeds can be achieved.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a high-resistance layer between the side of the ridge waveguide and the dielectric layer for improved optical mode propagation control while keeping a minimal capacitance of the waveguide for faster switching speeds.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sano, Soref and Huang and in view of Koui (US 5,918,109).

Regarding claim 16, Sano teaches a MQW ridge waveguide optical modulator (Fig.2A), including:

1) a semi-insulating semiconductor substrate (item 7) with a principal plane including a partially exposed surface,

2) an optical waveguide ridge disposed on the substrate that includes;

a) a first cladding layer of a first conductivity type (item 5-2),

b) an optical absorption layer (item 3), and

c) a second cladding layer of a second conductivity type (item 5-1),

3) the ridge has a side with a flat portion extending uniformly from the top of the ridge to the exposed surface of the semiconductor substrate,

4) a dielectric film (items 9-1 and 9-2) which covers the ridge and the substrate and which has a first opening at the top of the ridge,

5) a first electrode (item 10) disposed on the dielectric film and mounted through the first opening on the top of the ridge, extending on the flat portion of the side of the ridge while in contact with the dielectric layer, and having one end on the substrate at the exposed surface, and

6) a second electrode disposed on the semiconductor substrate.

Sano does not teach a second opening in the dielectric layer in a substrate surface region excluding the exposed surface region or a connection of the second electrode with the first cladding layer through the second opening in the dielectric layer.

Soref teaches of a ridge waveguide (Fig.2e) where a second opening in the outer dielectric layer allows the second electrode to contact the first cladding layer, rather than using a body contact on the underside of the substrate as taught by Sano. Soref further states that this method allows convenient access to the first cladding layer. Other advantages would be readily recognized by those skilled in the art, such as faster switching times, lower operating voltages, and simpler electrical connections. Soref does not teach the position of the opening to be on the substrate region.

Huang teaches the use of body electrodes being formed on the top of a substrate region through openings in the dielectric layer (Fig.3, contacting lower cladding layer 42 for modulator 50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to place the second electrode in contact with the first cladding layer on the substrate region. The placement of the second electrode on the same side of the substrate as the ridge waveguide provides simple, convenient electrical connection to the first cladding layer. Further, the teachings of Soref and Huang demonstrate obvious functional equivalents relating to the exact placement of the electrode, either making contact on top of the substrate region or along the side of the waveguide ridge. In either configuration, both make contact through an opening in the dielectric layer.

Further regarding claim 16 and regarding claim 17, Koui discloses a ridge semiconductor laser and a ridge waveguide optical modulator made on the same chip where both active regions of the devices are aligned along the same optical axis. In this way, more compact, efficient

optical circuits can be realized, just as conventional IC fabrication allowed very small electrical circuits to come into being. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make various optical components on the same chip for compactness and simplicity of manufacturing.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Terakado and Sano and in view of Koui.

Regarding claim 16, Terakado teaches the structure of a ridge waveguide optical modulator (Fig.1), including:

1) a semi-insulating semiconductor substrate (item 1) with a principal plane including a partially exposed surface,

2) an optical waveguide ridge disposed on the substrate that includes;

a) a first cladding layer of a first conductivity type (item 2),

b) an optical absorption layer (item 3), and

c) a second cladding layer of a second conductivity type (item 4),

3) the ridge has a side with a flat portion extending uniformly from the top of the ridge to the exposed surface of the semiconductor substrate,

4) a dielectric film (item 10) which covers the ridge and the substrate and which has a first opening at the top of the ridge and a second opening in a region of the substrate other than the exposed surface,

5) a first electrode (item 14) disposed on the dielectric film and mounted through the first opening on the top of the ridge and having one end on the substrate at the exposed surface, and

6) a second electrode disposed on the semiconductor substrate and connected to the first cladding layer through the second opening in the dielectric film.

Terakado does not disclose the first electrode being extended along the flat side of the ridge waveguide and in contact with the dielectric film.

Sano teaches the practice of a first electrode that is in contact with the dielectric film throughout it's extension along the flat portion of the ridge waveguide.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the electrode extension in contact with the dielectric layer because it is far easier to manufacture, with fewer steps, as opposed to the depositing and then etching the sacrificial layer that allows formation of the "air bridge" as disclosed in Terakado.

Further regarding claim 16 and regarding claim 17, Koui discloses a ridge semiconductor laser and a ridge waveguide optical modulator made on the same chip where both active regions of the devices are aligned along the same optical axis. In this way, more compact, efficient optical circuits can be realized, just as conventional IC fabrication allowed very small electrical circuits to come into being. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make various optical components on the same chip for compactness and simplicity of manufacturing.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hietala (US 5,270,532) and Revelli (US 5,276,745) teach the practice of connecting the first cladding layer to electrodes on the same side of the substrate as the ridge waveguide; Haase (US 5,165,105) teaches a top electrode deposited over the entire surface of the waveguide and substrate regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas R Artman whose telephone number is (703) 305-0203. The examiner can normally be reached on 8am - 5:30pm Monday - Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Kim can be reached on (703) 305-3492. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

Thomas R. Artman
Patent Examiner
May 13, 2003

ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
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